

Derivation of Eq. (15), and Design Details of the Compensator G_{c2} , the Rogowski Coil in the Paper

For clarification purposes, references to Fig. xx, Eq. (xx), TABLE xx in this document are alluding to the figures, equations, and tables from the paper titled "A Configurable DC-DC Ripple Attenuator Module with Active Ripple Cancellation Technique." Similarly, Fig. Axx, Eq. (Axx), TABLE Axx refer to the figures and equations in this document. The files xxx.sxsch and xxx.m respectively denote the SIMPLIS simulation file and MATLAB script codes supplied as supporting materials.

Note that: the simulations and codes mentioned in this *Readme.PDF* are solely intended to assist beginners in comprehending the relevant content of this document.

Part1. Derivation of Eq. (15)

1.1 Preparation Work

Taking $N=3$ as an example, the converter system in Fig. 2 operates in a three-phase interleaved mode, where one cycle (T_s) is divided into PHASE1, PHASE2, and PHASE3. During the operation of PHASEX, $X=\{1,2,3\}$, it can be further decomposed based on the rising and falling of the current i_{sum} , as illustrated in Fig. 3, into modes M1 and M2. The corresponding times for these modes are T_{effon} and T_{effoff} , with corresponding duty cycles D_{effon} and D_{effoff} . For $N=3$, the mode transitions of the converter system in Fig. 2 are depicted in Fig. A1.

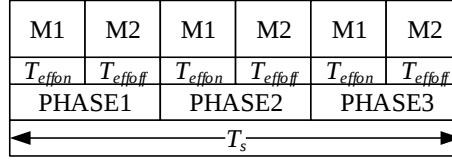


Fig. A1. The mode transitions of MBC with $N=3$.

Next, we will illustrate the derivation process using Eq. (15a) as an example. Eq. (15a) represents the transfer function of the output voltage v_o with respect to the duty cycle d_1 , denoted as G_{vod1} . Therefore, setting d_2 to zero in Fig. 7a results in Fig. A2(a) (similarly, setting d_1 to zero yields Fig. A2(b) for deriving G_{vod2}).

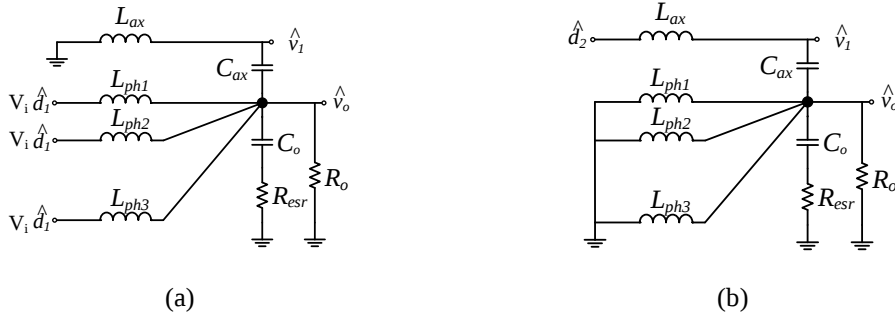
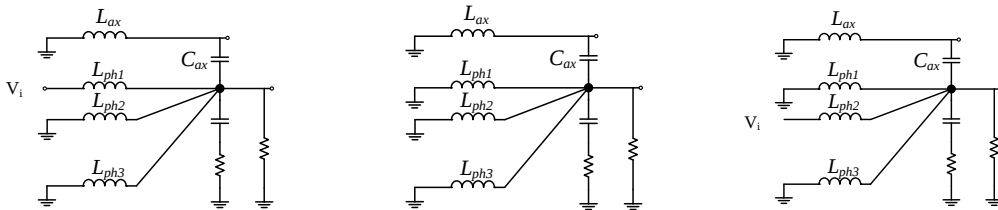


Fig. A2. Equivalent circuit used to derive transfer function. (a) G_{vod1} . (b) G_{vod2} .

According to Fig. A1, the circuit configurations for different modes in Fig. A2(a) are depicted in Fig. A3.



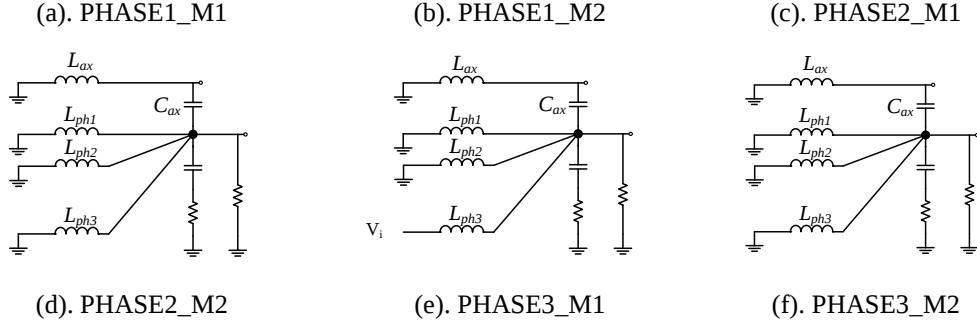


Fig. A3. MBC with RAM circuit in different modes.

From Fig. A3, it can be observed that Fig. A3(b), (d), (f) are identical. Simultaneously, based on the assumption in the paper that $L_{ax}=L_1=L_2=L_3=L$, Fig. A3(a), (c), (e) are also identical.

Considering the above analysis, the six modes in Fig. A3 can be simplified into two modes, namely M1 and M2, and their circuit diagrams are illustrated in Fig. A4.

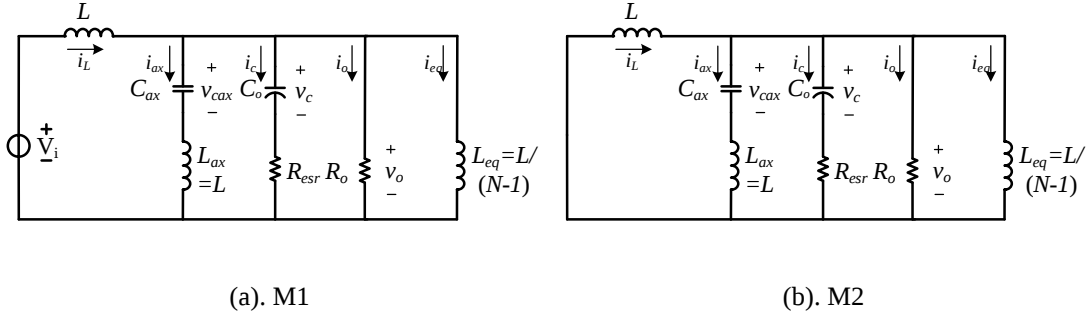


Fig. A4. Two simplified equivalent circuit diagrams of MBC with RAM.

1.2 Derivation Process

The two equivalent circuit diagrams in Fig. A4 will be utilized for state averaging. We now formally begin the derivation of G_{vod1} .

First, according to Fig. A4(a) and Fig A4(b), the differential equations of M1, M2 are listed, as shown in Eq. (A1). In the Eq. (A1), where $v_o = v_c + (i_L - i_{ax} - i_o - i_{eq})R_{esr}$, $i_o = \frac{v_o}{R_o}$.

$$\begin{cases} L \cdot \dot{i}_L = v_i(t) - v_o \\ L_{ax} \cdot \dot{i}_{ax} = v_o - v_{cax} \\ L_{eq} \cdot \dot{i}_{eq} = v_o \\ C_o \cdot \dot{v}_c = i_L - i_{ax} - i_o - i_{eq} \\ C_{ax} \dot{v}_{cax} = i_{ax} \end{cases}$$

(A1-1)

$$\begin{cases} L \cdot \dot{i}_L = -v_o \\ L_{ax} \cdot \dot{i}_{ax} = v_o - v_{cax} \\ L_{eq} \cdot \dot{i}_{eq} = v_o \\ C_o \cdot \dot{v}_c = i_L - i_{ax} - i_o - i_{eq} \\ C_{ax} \dot{v}_{cax} = i_{ax} \end{cases}$$

(A1-2)

Second, the differential equations are rewritten as a matrix form, Eq. (A2):

$$\begin{aligned} \mathbf{k}\dot{\mathbf{x}}(t) &= \mathbf{A}_m \mathbf{x}(t) + \mathbf{B}_m \boldsymbol{\mu}(t) \quad m=1,2 \\ \mathbf{y} &= \mathbf{C} \cdot \mathbf{x}(t) \end{aligned} \quad (\text{A2})$$

$$\begin{cases} \mathbf{x}(t) = [i_L \quad i_{ax} \quad i_{eq} \quad v_c \quad v_{cax}]^T \\ \mathbf{k} = \text{diag}[L \quad L_{ax} \quad L_{eq} \quad C_o \quad C_{ax}] \\ \boldsymbol{\mu}(t) = [v_i(t) \quad 0 \quad 0 \quad 0 \quad 0]^T \end{cases}$$

Third, by averaging the state space matrix of two modes, we get the average model constituting circuit description matrix $\mathbf{A}$, input matrix $\mathbf{B}$, and output matrix $\mathbf{C}$, as shown in Eq. (A3), Eq. (A4), and Eq. (A5). As from Fig. A4, when switching circuits transfer from M1 to M2, only the voltage source changes, which means that both the circuit description matrix $\mathbf{A}_1$ and $\mathbf{A}_2$ are equal to $\mathbf{A}$.

$$\begin{aligned} \mathbf{A} &= N(D_{eff} \mathbf{A}_1 + D'_{eff} \mathbf{A}_2) = \mathbf{A}_1 = \mathbf{A}_2 \\ &= \begin{bmatrix} \frac{-R_o R_{esr}}{R_o + R_{esr}} & \frac{R_o R_{esr}}{R_o + R_{esr}} & \frac{R_o R_{esr}}{R_o + R_{esr}} & \frac{-R_o}{R_o + R_{esr}} & 0 \\ \frac{R_o R_{esr}}{R_o + R_{esr}} & \frac{-R_o R_{esr}}{R_o + R_{esr}} & \frac{-R_o R_{esr}}{R_o + R_{esr}} & \frac{R_o}{R_o + R_{esr}} & -1 \\ \frac{R_o R_{esr}}{R_o + R_{esr}} & \frac{-R_o R_{esr}}{R_o + R_{esr}} & \frac{-R_o R_{esr}}{R_o + R_{esr}} & \frac{R_o}{R_o + R_{esr}} & 0 \\ \frac{R_o}{R_o + R_{esr}} & \frac{-R_o}{R_o + R_{esr}} & \frac{-R_o}{R_o + R_{esr}} & \frac{-1}{R_o + R_{esr}} & 0 \\ 0 & 1 & 0 & 0 & 0 \end{bmatrix} \end{aligned} \quad (\text{A3})$$

$$\begin{aligned} \mathbf{B} &= N(D_{eff} \mathbf{B}_1 + D'_{eff} \mathbf{B}_2) = [ND_{eff} \quad 0 \quad 0 \quad 0 \quad 0]^T \\ \mathbf{B}_1 &= [1 \quad 0 \quad 0 \quad 0 \quad 0]^T \quad \mathbf{B}_2 = [0 \quad 0 \quad 0 \quad 0 \quad 0]^T \end{aligned} \quad (\text{A4})$$

$$\mathbf{C} = \begin{bmatrix} \frac{R_o R_{esr}}{R_o + R_{esr}} & \frac{-R_o R_{esr}}{R_o + R_{esr}} & \frac{-R_o R_{esr}}{R_o + R_{esr}} & \frac{R_o}{R_o + R_{esr}} & 0 \end{bmatrix} \quad (\text{A5})$$

$$\mathbf{k} \frac{d\hat{\mathbf{x}}(t)}{dt} = \mathbf{A}\hat{\mathbf{x}}(t) + \mathbf{B}\hat{\boldsymbol{\mu}}(t) + \mathbf{M}\hat{\mathbf{d}}(t) \quad (\text{A6})$$

Fourth, write the small signal AC model equation Eq. (A6), in Eq. (A6) matrix $\mathbf{M}$ can be calculated by equation Eq. (A7).

$$\begin{aligned} \mathbf{M} &= N(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + N(\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U} \\ &= [N \cdot V_i \quad 0 \quad 0 \quad 0 \quad 0]^T \end{aligned} \quad (\text{A7})$$

Finally, by putting the $\mathbf{B}$ or $\mathbf{M}$ matrix to zero respectively in the small-signal AC model equation Eq. (A6), the transfer function from control to output G_{vodi} Eq. (A8-1) and from input to output G_{vovi} Eq. (A8-2) can be obtained.

$$\mathbf{G}(s) \Big|_{\frac{\hat{v}_o}{\hat{d}_i}} = \mathbf{C}(s\mathbf{I} - \mathbf{k}^{-1}\mathbf{A})^{-1}\mathbf{k}^{-1}\mathbf{M} \quad (\text{A8-1})$$

$$\mathbf{G}(s) \Big|_{\frac{\hat{v}_o}{\hat{v}_i}} = \mathbf{C}(s\mathbf{I} - \mathbf{k}^{-1}\mathbf{A})^{-1}\mathbf{k}^{-1}\mathbf{B} \quad (\text{A8-2})$$

1.3 Explanations and Notes

The derivation related to Eq. (13a) can be cross-referenced with the content in 7.3 *State-Space Averaging* in "*Fundamentals of Power Electronics Second Edition*"[1]. Interestingly, in Eq. (A3), Eq. (A4), and Eq. (A7) of this document, the treatment of matrices $\mathbf{A}$, $\mathbf{B}$, and $\mathbf{M}$, as rewrite in Eq. (A9-2), differs from the treatment approach in the reference book, *specifically in Eq. (7.93) and Eq. (7.96) in [1]*. The Eq. (7.93), and the $\mathbf{M}$ in Eq. (7.96) in the reference book are also extracted, and rewrite in Eq. (A9-1).

$$\begin{cases} \mathbf{A} = D\mathbf{A}_1 + D'\mathbf{A}_2 \\ \mathbf{B} = D\mathbf{B}_1 + D'\mathbf{B}_2 \\ \mathbf{M} = (\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U} \end{cases}$$

(A9-1)

$$\begin{cases} \mathbf{A} = N(D_{eff}\mathbf{A}_1 + D'_{eff}\mathbf{A}_2) \\ \mathbf{B} = N(D_{eff}\mathbf{B}_1 + D'_{eff}\mathbf{B}_2) \\ \mathbf{M} = N(\mathbf{A}_1 - \mathbf{A}_2)\mathbf{X} + N(\mathbf{B}_1 - \mathbf{B}_2)\mathbf{U} \end{cases}$$

(A9-2)

The reason for the discrepancy is as follows:

When the $N=1$, there are just two modes in buck converter. Eq. (7.96) is its state equations of the small-signal ac model, as rewrite in Eq. (A10) (*extracted from the reference book*).

$$\mathbf{k} \frac{d(\mathbf{X} + \hat{\mathbf{x}}(t))}{dt} = [(D + \hat{d}(t))\mathbf{A}_1 + (D' - \hat{d}(t))\mathbf{A}_2](\mathbf{X} + \hat{\mathbf{x}}(t)) + [(D + \hat{d}(t))\mathbf{B}_1 + (D' - \hat{d}(t))\mathbf{B}_2](\mathbf{U} + \hat{\mathbf{u}}(t))$$

(A10)

In the case of N phases, there are a total of $2N$ modes. Taking $N=3$ as an example, there are a total of 6 modes as illustrated in Fig. A1. The state equations of the small-signal ac model are as follows:

$$\begin{aligned} \mathbf{k} \frac{d(\mathbf{X} + \hat{\mathbf{x}}(t))}{dt} &= [(D_{eff} + \hat{d}(t))\mathbf{A}_1 + (D'_{eff} - \hat{d}(t))\mathbf{A}_2]N(\mathbf{X} + \hat{\mathbf{x}}(t)) + [(D_{eff} + \hat{d}(t))\mathbf{B}_1 + (D'_{eff} - \hat{d}(t))\mathbf{B}_2]N(\mathbf{U} + \hat{\mathbf{u}}(t)) \\ &= [(D_{eff}\mathbf{A}_1 + D'_{eff}\mathbf{A}_2)N\mathbf{X} + (D_{eff}\mathbf{B}_1 + D'_{eff}\mathbf{B}_2)N\mathbf{U}] + [(D_{eff}\mathbf{A}_1 + D'_{eff}\mathbf{A}_2)N]\hat{\mathbf{x}}(t) + [(D_{eff}\mathbf{B}_1 + D'_{eff}\mathbf{B}_2)N]\hat{\mathbf{u}}(t) + [(\mathbf{A}_1 - \mathbf{A}_2)N\mathbf{X} + (\mathbf{B}_1 - \mathbf{B}_2)N\mathbf{U}]\hat{d}(t) + \text{nonlinear_terms} \end{aligned}$$

(A11)

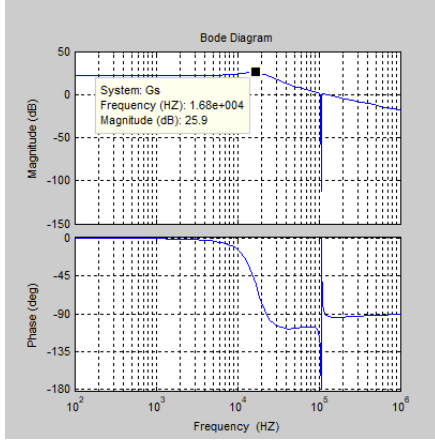
Due to the fact that the derivative $d\mathbf{X}/dt$ is zero, $\mathbf{k} \frac{d(\mathbf{X} + \hat{\mathbf{x}}(t))}{dt} = \mathbf{k} \frac{d(\hat{\mathbf{x}}(t))}{dt}$, neglecting the higher-order nonlinear terms in Eq. (A11), and contrasting it with the standard form depicted in Eq. (A6) yields the result presented in Eq. (A9-2).

Another interesting thing is that $\mathbf{A} = N(D_{eff}\mathbf{A}_1 + D'_{eff}\mathbf{A}_2) \neq N\mathbf{A}_1/N\mathbf{A}_2$.

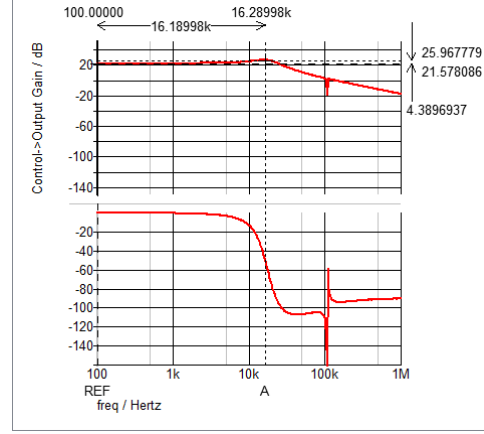
This arises because for $N=1$, there is $D + D' = 1$, whereas for three-phase operation with $N=3$, there is $(D_{eff} + D'_{eff})N = 1$.

1.4 Comparison of MATLAB Script and SIMPLIS Simulation Results

The author has uploaded the attachments "[20231130Gvod1.sxsch](#)" (directory: \SCH&SIMPLIS&MATLAB\SIMPLIS SIMULATION\Gvod1\) and "[Gvod1_1201.m](#)" (directory: \SCH&SIMPLIS&MATLAB\MATLAB\), serving as supporting materials. The input parameters for these materials are provided in [TABLE I of the paper](#). The MATLAB script "[Gvod1_1201.m](#)" encapsulates the derivation process for Eq. (15a), and with slight modifications, it can be applied to derive formulas Eq. (15b) and Eq. (15c). "[20231130Gvod1.sxsch](#)" is used for simulation to obtain the transfer function, which helps to support derivation process of "[Gvod1_1201.m](#)". The results of the transfer functions obtained from these two files are depicted in Fig. A5:



(a). Calculate result.



(b). Simulation result.

Fig. A5. Results supporting the derivation process for Eq. (15a).

From Fig. A5, it can be observed that, neglecting the influence of damping, the two curves are nearly identical. This is due to the fact that the simulation file includes the on-state resistance of the switching devices, while the MATLAB script neglected the parasitic resistances in series with the L_{ax} and C_{ax} branches, resulting in different attenuation at the f_{osc} (f_{osc} refer to Eq. (16) in the paper) frequency in the magnitude plot.

Part2. Design of Compensator G_{c2} for the Prototype

2.1 Design of Compensator G_{c2}

Based on the conclusions drawn from Fig. 11 in paper, it is inferred that Eq. (15c), $F_s G_{v1d2}$, can be approximated by Eq. (18), $F_s G'_{v1d2}$. Its characteristics closely resemble the transfer function of a non-loaded buck converter. Therefore, the design of this compensator can be approached using the parameter design method outlined in *AN-1162.PDF*, referenced in the paper as [23], which introduces the design of a TYPE III-B compensator [2].

The typically type III compensation network which is used for a voltage-mode PWM converter is shown in Fig. A6.

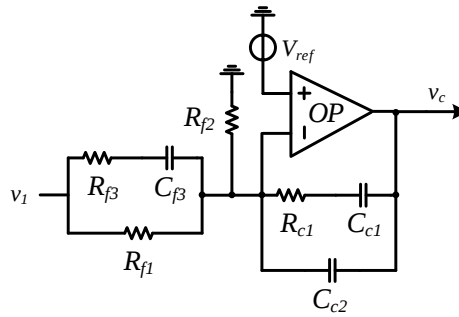


Fig. A6. Circuit diagram of TYPE III compensator.

When capacitance of $C_{c2} \ll$ that of C_{c1} , the transfer function of TYPE III-B compensator can be simplified to Eq. (A12).

$$H(s) \approx - \frac{(1 + R_{c1}C_{c1} \cdot s) [1 + s \cdot C_{f3}(R_{f1} + R_{f3})]}{s \cdot R_{f1}C_{c1}(R_{c1}C_{c2} \cdot s + 1)(R_{f3}C_{f3} \cdot s + 1)} \quad (A12)$$

The compensator has two zeros and three poles as given below:

$$\begin{cases} F_{z1} = \frac{1}{2\pi R_{c1} C_{c1}} & F_{z2} = \frac{1}{2\pi C_{f3} (R_{f1} + R_{f3})} \\ F_{p3} = \frac{1}{2\pi R_{c1} C_{c2}} & F_{p1} = 0 & F_{p2} = \frac{1}{2\pi R_{f3} C_{f3}} \end{cases} \quad (A13)$$

If the zero caused by the ESR is above half of the switching frequency, that is if Eq. (A14) is valid, Type III-B compensation method is used. Condition Eq. (A14) happens when MLCC capacitors are used at the C_{ax} of the RAM.

$$\begin{cases} F_{LC} < F_0 < F_s / 2 < F_{ESR} \\ F_{LC} = \frac{1}{2\pi \sqrt{L_{ax} C_{ax}}} \\ F_{ESR} = \frac{1}{2\pi R_{cax_esr} C_{ax}} \end{cases} \quad (A14)$$

Typically, F_0 , the zero crossover frequency can be set to 1/10~1/5 of the switching frequency F_s (corresponding to the ripple frequency f_r in paper). The speed of the system response to output voltage transients is determined by F_0 . In other words, the higher the crossover frequency, the faster transient response would be.

If this happens, the poles and zeros of the compensator will be placed as follows:

$$\begin{cases} F_{z1} = \frac{F_{z2}}{2} & F_{z2} = F_0 \sqrt{\frac{1 - \sin \theta}{1 + \sin \theta}} \\ F_{p3} = \frac{F_s}{2} & F_{p1} = 0 & F_{p2} = F_0 \sqrt{\frac{1 + \sin \theta}{1 - \sin \theta}} \end{cases} \quad (A15)$$

Theta, θ , is chosen to be 45° in paper and this is about the maximum practical phase-lead obtainable from a lead compensator, which is relative to phase margin of loop gain $T(s)$. The crossover frequency F_0 is set to be 1/8 of the ripple frequency f_r , $F_0 = N \cdot 300 \text{ kHz} / 8 = 112.5 \text{ kHz}$ ($N=3$). The f_{osc} in paper is equal to about 1/30 of the f_r . The f_{osc} in paper is equal to the F_{LC} in this document.

By simultaneously solving Eq. (A13) and Eq. (A15), one can obtain the resistor and capacitor values for the compensator. The author has developed a MATLAB script file, "Gc2_1201.m," based on this design method. This script can compute the results shown in Fig. 12 of the paper using the parameters: theta=45°, $F_0 = f_r / 8 = 900 \text{ kHz} / 8 = 112.5 \text{ kHz}$, and $F_{LC} = 30 \text{ kHz}$.

In experiments and simulations, the following parameters were used to calculate the corresponding resistor and capacitor values for the G_{c2} compensator (using the .sxsch files):

- For [20230921\(PhaseMargin45\).sxsch](#): theta=45, $F_0 = f_r / 6 = 900 \text{ kHz} / 6 = 150 \text{ kHz}$, $F_{LC} = 30 \text{ kHz}$.
- For [20230921\(PhaseMargin75\).sxsch](#): theta=75, $F_0 = f_r / 6 = 900 \text{ kHz} / 6 = 150 \text{ kHz}$, $F_{LC} = 30 \text{ kHz}$.

2.2 Impact of Loop2's Phase Margin on MBC Transient Response

The author has provided two simulation files, namely, "[20230921\(PhaseMargin75\).sxsch](#)" and "[20230921\(PhaseMargin45\).sxsch](#)," intended for comparing the impact of different phase margin settings on the transient of the converter. It's important to note that the actual startup behavior of the prototype depends on the start-up control scheme by the chip used in the prototype. These simulation files are only intended to illustrate that the feedback loops of RAM and MBC can operate normally under general conditions.

In conclusion, there is still room for improvement in the feedback loop of the G_{c2} controller. However, both simulation and experimental results indicate that the insertion of RAM does not affect the stability of MBC.

Finally, in the prototype, the RAM adopts the PhaseMargin75 design. However, due to the larger output capacitance (prototype, $C_o=2450$ uF) compared to the simulation (simulation, $C_o=1000$ uF), the capacitance and resistance values in the Type-III compensator were recalculated, as detailed in [SCH_RAM.PDF](#) (directory: \SCH&SIMPLIS&MATLAB\SCHEMATIC\).

Part3. Can Inserting RAM Reduce the Output Capacitance of the System?

3.1 Background

The author believes that electrolytic capacitors are still necessary in certain applications, such as bulk energy storage and providing the hold-on time of converters. Therefore, the research subject is chosen as extending the lifespan of electrolytic capacitors. (In deed, the author have repaired numerous low-cost electronic devices, and during the repairs, he found that DC-DC converters are prone to damage, due to the aging of electrolytic capacitors).

3.2 Simulation Results

Back to the question, can inserting RAM reduce the output capacitance of the system? The author thinks that it is feasible in theory (On the premise that only the filtering function of the capacitor is caring), and one of the major functions of this kind of ripple canceller circuit is to realize the electrolytic capacitor-less of the converter. That is to say, MLCC capacitor with small capacitance is used to replace bulk electrolytic capacitor, and there are many existed literatures available for reference.

At the same time, the author can also provide a simulation file as proof. Readers can try to adjust the value of C_o in [20230921 \(phase margin 45\).sxch](#) or [20230921\(PhaseMargin75\).xsch](#) and configure jumper J2 to compare the experimental results between MBC with and without inserting RAM.

Fig. A9 shows the comparison results of the output voltage ripple obtained through [20230921 \(phase margin 45\).sxch](#) The output capacitors are configured as $C_o=1000$ uF and $C_o= 100$ uF, and the ESR is 5mR (this parameter is selected only for convenience, and readers can modify it by themselves).

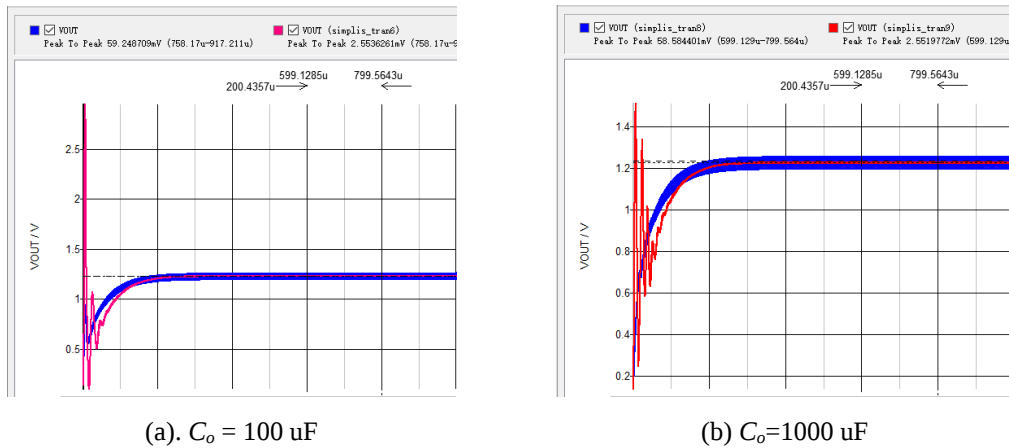


Fig. A9. Close loop simulation results in different C_o .

The corresponding simulation results for Fig. A9 are summarized in TABLE. AI. From the results in the TABLE AI, it can be observed that the capacitance value does not significantly affect the magnitude of voltage ripple. The primary contribution for the voltage ripple is caused by the Equivalent Series Resistance (ESR= 5mR). Based on the simulation results, it can be concluded that the RAM can reduce the output voltage ripple by decreasing the output current ripple.

Therefore, the author suggests that theoretically replacing electrolytic capacitors with MLCC is feasible.

TABLE. AI		
RAM state	$C_o=100\text{ }\mu\text{F}$, $\text{esr}=5\text{ mR}$	$C_o=1000\text{ }\mu\text{F}$, $\text{esr}=5\text{ mR}$
Plugged	$V_{pp}=2.55\text{ mV}$	$V_{pp}=2.55\text{ mV}$
Un-Plugged	$V_{pp}=59.25\text{ mV}$	$V_{pp}=58.58\text{ mV}$

3.3 Notes and Interesting Observations

1) Arbitrarily modifying C_o in the simulation is not rigorous, as with changes in C_o , the design of feedback controller G_{cl} should also be reconfigured.

2) The attenuation of voltage ripple in the actual prototype is not as ideal as in the simulation. The author guesses two possible reasons:

- Reason 1: The output current ripple is not completely eliminated.
- Reason 2: There seems to be an impact of parasitic parameters (and possibly even the influence of mutual inductance).

3) If a converter's C_o play a role in energy storage, inserting RAM can't reduce the C_o values of the system.

Part.4 Explanation of Rogowski Coil Design Issues

4.1 Role Played in the Prototype

Essentially, the Rogowski coil in the prototype is served as a current sensor, and therefore, any form of current sensor can be used as a replacement for the Rogowski coil (before that a redesign of the ATC is needed). The author chose the Rogowski coil as the current sensor for this project based on the following reasons [3]:

- Very high bandwidth enabling for example the measurement of switching transients in semiconductors
- Capability of measuring large currents. The same size coil can be used for measuring 100 A or 100 kA whereas other current transducers increase in size for increasing current magnitude.
- Non-saturation. The coil is not damaged by overcurrent.
- Isolation
- Ease of use. The coil can be relatively thin and flexible enabling it to be clipped around a conductor or current carrying device.
- Non-intrusive. There is no discernable loading of the circuit carrying the current to be measured and the injected impedance is typically a few pH.
- Very good linearity due to absence of magnetic materials.

4.2 Design of Rogowski Coil Parameters

The specific design details have been provided in the paper, and we designed it using a manual winding method. Readers may question the expensive cost of Rogowski coil current probes and the feasibility of hand-winding coils. At least in the prototype, it is feasible, and there are precedents to draw upon, as mentioned in [4]: "However, provided the coil is single layer closely wound, it can be wound quite acceptably by hand."

The Rogowski principle has been known since 1912. If a uniform coil is wound on a non-magnetic former of constant cross-section area and shaped into a closed loop, then the voltage induced in the coil is directly proportional to the rate of change of current I passing through the loop according to the equation Eq. (A16).

$$e = \mu_0 N A \frac{di}{dt} = M \frac{di}{dt} \quad (\text{A16})$$

Where, e is the induced voltage (V), N is the turns density (turns/m), A is the turn area (m^2), and μ_0 represents the magnetic permeability in a vacuum, $\mu_0 = 4\pi \times 10^{-7}$ (H/m).

From Eq. A16, the mutual inductance M in Eq. (26) can be calculated using Eq. (A17).

$$M = \mu_0 N A \quad (\text{A17})$$

By substituting the coil parameters from the paper: $N = 200/4 \text{ cm} = 200/(0.04 \text{ m}) = 5000$, $A = (0.002 \text{ m}/2)^2 \pi = 3.14 \times 10^{-6}$ into Eq. (A16), the calculation yields $M = 20 \text{ nH}$. Then, substituting $M = 20 \text{ nH}$, $V_i = 12$, $L = 220 \text{ nH}$ into Eq. (26) gives $\Delta V_{CT} \approx 1 \text{ V}$. This is close to the experimental result $\Delta V_{CT} \approx 800 \text{ mV}$ shown in Fig. 17 of the paper.

Possible reasons for the discrepancy between theoretical calculation and experimental measurement:

- 1) Inconsistency in the parameters of hand-wound Rogowski coils.
- 2) The position of the coil and the conductor under measured [5].

4.3 How to Hand-Wind a Rogowski Coil

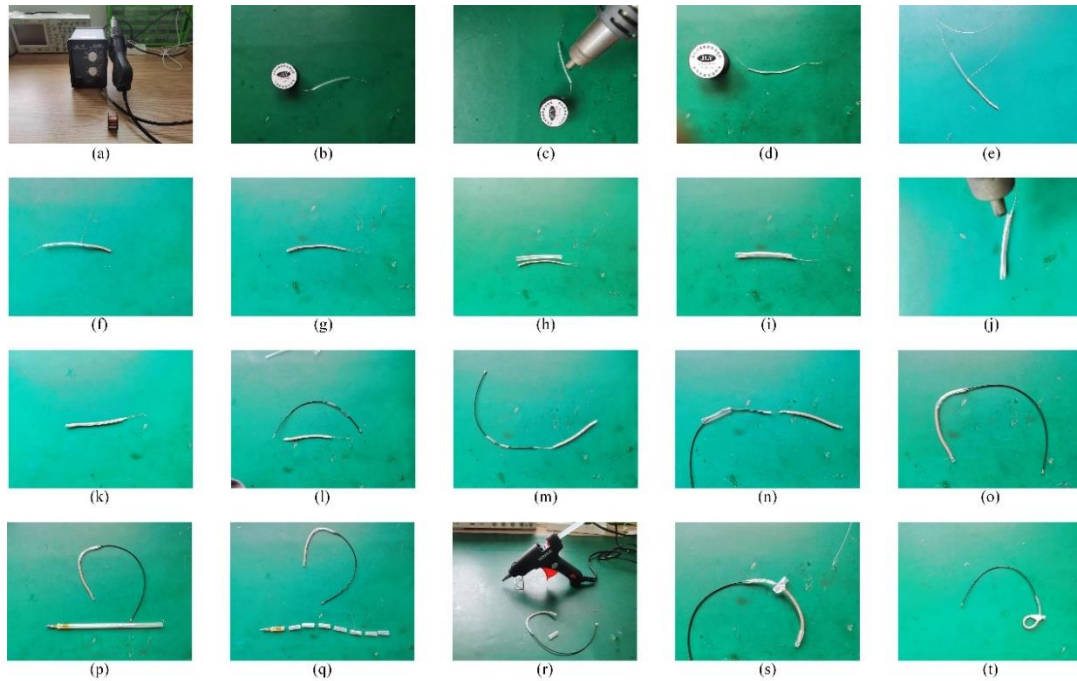


Fig. A10. Images showing how I make the Rogowski Coil sensor.

(a) Materials needed: One spool of 0.1 mm diameter enameled wire, one 5 cm long heat-shrink tube.

(b) Insert the heat-shrink tube into the enameled wire.

(c) Heat the heat-shrink tube with a hot air gun to make it shrink.

(d) Image of the shrunken heat-shrink tube. You can control the coil diameter by repeating steps (b) and (c).

(e) Hand-wind the coil.

(f) Push the uneven coil to the right side to make it more compact.

(g) Semi-finished coiled product.

(h) Need a larger diameter heat-shrink tube.

(i) Insert the larger diameter heat-shrink tube into the semi-finished coil.

- (j) Use a hot air gun to heat the heat-shrink tube, making it shrink.
- (k) Image of the shrunken heat-shrink tube. The larger diameter heat-shrink tube is used to protect the coil structure.
- (l) Prepare an IPEX cable.
- (m) Weld the IPEX cable and the Rogowski coil.
- (n) Use a smaller heat-shrink tube to wrap the welded area for insulation.
- (o) Use a thicker heat-shrink tube to reinforce the connection between the coil and the IPEX cable.
- (p) Prepare a used neutral pen core.
- (q) Cut it into small plastic tubes.
- (r) Take a small piece of the plastic tube and prepare a glue gun.
- (s) Use the glue gun to secure the plastic tube onto the coil.
- (t) Completion.

4.4 Impact of Coil Errors

Is the manufactured error in a manual winding coils affect the stable operation of the system?

Conclusion: Assuming this coil sensor is used in a current probe, errors can have a significant impact. In current probes, the coil must consider the smoothness of the amplitude-frequency characteristics and phase-frequency characteristic curves. However, in this system, the impact of these errors is insignificant.

Reason 1: The system focuses only on the amplitude of the v_{CT} signal output at the f_r . As long as Δv_{CT} is greater than the comparator's noise, and a larger signal is preferable.

Reason 2: The role of the Rogowski coil in this system is to provide timing synchronization for the RAM and MBC. A well-wound coil has a fixed phase-frequency curve, and the delay at a certain frequency point is also fixed. We designed a monostable trigger for delay compensation. Thus, even if there is a signal delay, it can be compensated.

Reason 3: What about the amplitude? The output signal amplitudes Δv_{CT} and v_{CTmid} from arbitrarily wound coils are inconsistent. To address this, we designed the ATC. Additionally, in the actual circuit, we added bias-adjusting potentiometer RP1 to the ATC, as shown in Fig. A11, sourced from the schematic [SCH_RAM.pdf](#). Compared to Fig. 6, we added a sliding potentiometer RP1 to flexibly adjust v_{CTmid} to compensate for parameter variations brought by manually wound coils.

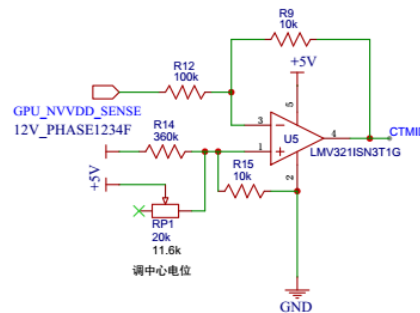


Fig. A11. Circuit diagram of ATC in prototype.

Part.5 Power Loss Analysis of Proposed System

5.1 Some Experimental Measurement Results

A thermal imaging camera is used to identify the hot spot in proposed system, as shown in Fig. A12. The results indicated significant losses in the in the switching transistor and the power inductor. Another

notable heat source was the LDO auxiliary power supply.

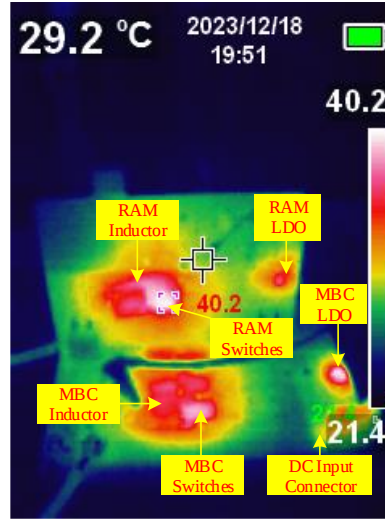
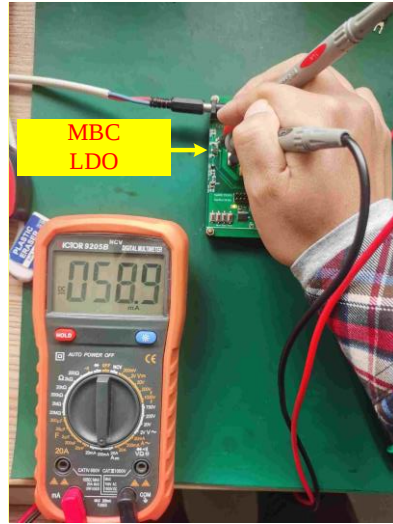


Fig. A12. Thermal image of MBC with RAM.

Measurement of BIAS losses P_{BIAS} :

This includes losses from the controller (up9511), microcontroller (hk32f030m4fp6), driver, and auxiliary circuits. Due to the use of an LDO for the auxiliary power supply (78L05), which generates significant heat, the bias current $I_{BIAS_MBC} = 58.9$ mA was measured. With an input voltage V_i of 12 V, the calculated $P_{BIAS_MBC} \approx 0.72$ W. These losses encompass the driver losses, as the driver chip is also powered through the LDO. The measured current was 60mA under no load, only slightly different from 58.9 mA under load.

Similarly, after disconnecting the filter inductor before RAM LDO (78L05), the measured input current $I_{BIAS_RAM} = 50$ mA, as shown in Fig. A13(b). With an V_i of 12V, the calculated $P_{BIAS_RAM} = 0.6$ W.



(a). I_{BIAS_MBC} .



(b). I_{BIAS_RAM} .

Fig. A13. I_{BIAS} measurements.

5.2 Definitions in Loss Analysis

The remaining losses can be estimated using the method provided in [6]. The variables are defined as follows:

Current-related:

$I_{IND_M_RMS}$: RMS current through the MBC power inductor.

$I_{IND_R_RMS}$: RMS current through the RAM power inductor.

$I_{IND_M_PP}$: Peak-to-peak current through the MBC power inductor.

$I_{IND_R_PP}$: Peak-to-peak current through the RAM power inductor.

$I_{Q2_M_RMS}$: RMS current through the lower switch of the MBC.

$I_{Q1_M_RMS}$: RMS current through the upper switch of the MBC.

$I_{Q2_R_RMS}$: RMS current through the lower switch of the RAM.

$I_{Q1_R_RMS}$: RMS current through the upper switch of the RAM.

The formulas for their calculations are given as follows:

$$I_{IND_M_PP} = \Delta i_{PHX} = \frac{V_i - V_o}{Lf_s} * D$$

$$I_{IND_R_PP} = \Delta i_{sum}$$

$$I_{IND_M_RMS} = \sqrt{\frac{I_o^2}{N^2} + \frac{\Delta i_{PHX}^2}{12}}$$

$$I_{IND_R_RMS} = \sqrt{\frac{\Delta i_{sum}^2}{12}}$$

$$I_{Q1_M_RMS} = I_{IND_M_RMS} \sqrt{D}$$

$$I_{Q2_M_RMS} = I_{IND_M_RMS} \sqrt{1-D}$$

$$I_{Q1_R_RMS} = I_{IND_R_RMS} \sqrt{1-D_{eff}}$$

$$I_{Q2_R_RMS} = I_{IND_R_RMS} \sqrt{D_{eff}}$$

Resistance-related:

R_{LxM} represents the equivalent resistance of the power inductor in MBC.

R_{LxR} represents the equivalent resistance of the power inductor in RAM.

R_{Q1M} represents the ON-state resistance of the upper switch in MBC.

R_{Q2M} represents the ON-state resistance of the lower switch in MBC.

R_{Q1R} represents the ON-state resistance of the upper switch in RAM.

R_{Q2R} represents the ON-state resistance of the lower switch in RAM.

Time-related:

T_{on} represents the turn-on time of the upper switch.

T_{off} represents the turn-off time of the upper switch.

Capacitance-related:

$C_{Q1,oss}$ represents the C_{oss} capacitance of the upper switch in MBC.

C_{SNBM} represents the snubber capacitance on the switching points in MBC.

C_{SNBR} represents the snubber capacitance on the switching points in RAM.

Voltage-related:

$V_{Q1,DS}$: Voltage for measuring the C_{oss} capacitance of upper switch, obtained from the datasheet.

V_D : Voltage drop of the parasitic diode in Q2.

5.3 Power Loss of MBC

1). Losses in the input and output filter section, including losses in the power inductors (P_{Lx_MBC}) and the filter capacitors (P_{Co}, P_{Ci}). P_{Co} , and P_{Ci} were estimated based on the results of thermal imaging. P_{Lx_MBC} can be calculated using Eq. (A18).

$$P_{Lx_MBC} = R_{LxM} * I_{IND_M_RMS}^2 \quad (A18)$$

2). Losses in the MBC low-side MOSFET, P_{Q2} . The P_{Q2} include conduction loss (P_{Q2M_1}), switching loss (P_{Q2M_2}), and body diode conduction loss (P_{Q2M_3}). P_{Q2M_3} is neglected due to the small dead time. P_{Q2M_1} and P_{Q2M_2} can be calculated using Eq. (A19) and Eq. (A20).

$$P_{Q2M_1} = R_{Q2M} * I_{Q2_M_RMS}^2 \quad (A19)$$

$$P_{Q2M_2} = V_D f_s \left[\left| \frac{I_o}{N} - \frac{\Delta i_{PHX}}{2} \right| \frac{t_{on}}{2} + \left(\frac{I_o}{N} + \frac{\Delta i_{PHX}}{2} \right) \frac{t_{off}}{2} \right] \quad (A20)$$

3). Losses in the MBC high-side MOSFET, P_{Q1} . The P_{Q1} include conduction loss (P_{Q1M_1}), switching loss (P_{Q1M_2}), and C_{oss} capacitor loss (P_{Q1M_3}), as shown in Eq. (A21-A23), with Eq. (A23) existed only when the converter operate in CCM condition (for example: $\frac{I_o}{N} - \frac{\Delta i_{PHX}}{2} > 0$).

$$P_{Q1M_1} = R_{Q1M} * I_{Q1_M_RMS}^2 \quad (A21)$$

$$P_{Q1M_2} = V_i f_s \left[\left| \frac{I_o}{N} - \frac{\Delta i_{PHX}}{2} \right| \frac{t_{on}}{2} + \left(\frac{I_o}{N} + \frac{\Delta i_{PHX}}{2} \right) \frac{t_{off}}{2} \right] \quad (A22)$$

$$P_{Q1M_3} \approx \frac{2V_i^{1.5} C_{Q1,OSS} f_s \sqrt{V_{Q1,DS}}}{3} \quad (A23)$$

4). Q_G losses in the MBC: this is already included in P_{BIAS_MBC} , is not recalculated.

5). Calculation of losses in the RC snubber, as shown in Eq. (A24).

$$P_{SNBM} = C_{SNBM} * f_s * V_i^2 \quad (A24)$$

The total losses can be estimated using Eq. (A25).

$$P_{TOT_MBC} \approx P_{BIAS_MBC} + N(P_{Lx_MBC} + P_{Q1M} + P_{Q2M} + P_{SNBM}) \quad (A25)$$

5.4 Power Loss of RAM

1). Losses in the RAM power inductors P_{Lx_RAM} can be calculated using Eq. (A26).

$$P_{Lx_RAM} = R_{LxR} * I_{IND_R_RMS}^2 \quad (A26)$$

2). Losses in the RAM low-side MOSFET, P_{Q2R} . Neglecting the body diode conduction loss (small dead time), the conduction loss (P_{Q2R_1}) and switching loss (P_{Q2R_2}) can be calculated using Eq. (A27) and (A28).

$$P_{Q2R_1} = R_{Q2R} * I_{Q2_R_RMS}^2 \quad (A27)$$

$$P_{Q2R_2} = V_D f_{eff} (I_{IND_R_PP} / 2)(t_{on} + t_{off}) / 2 \quad (A28)$$

3). Losses in the RAM high-side MOSFET, P_{Q1R} . The losses include conduction loss (P_{Q1R_1}) and turn-off loss (P_{Q1R_2}), as shown in Eq. (A29-A30).

$$P_{Q1R_1} = R_{Q1R} * I_{Q1R_R_RMS}^2 \quad (A29)$$

$$P_{Q1R_2} = V_i f_{eff} [(\frac{\Delta i_{sum}}{2}) \frac{t_{off}}{2}] \quad (A30)$$

4). Q_G losses in the RAM: this is already included in P_{BIAS_RAM} , is not recalculated.

5). Calculation of losses in the RC snubber, as shown in Eq. (A31).

$$P_{SNBR} = C_{SNBR} * f_{eff} * V_i^2 \quad (A31)$$

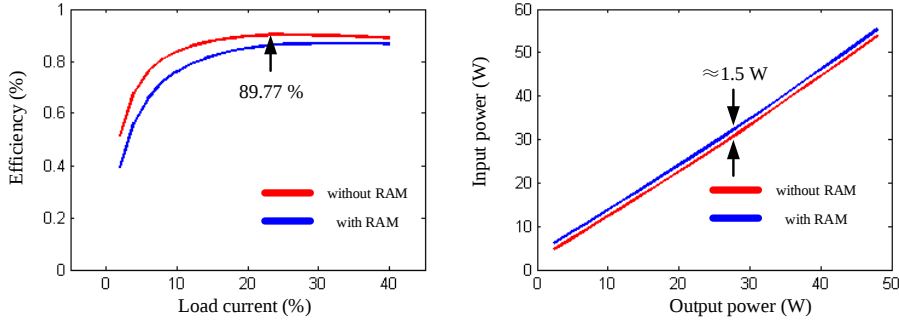
The total losses can be estimated using Eq. (A32).

$$P_{TOT_RAM} \approx P_{BIAS_RAM} + (P_{Lx_RAM} + P_{Q1R} + P_{Q2R} + P_{SNBR}) \quad (A32)$$

5.5 Results and Improvements from Loss Analysis

For simplify, the author organized the code into MATLAB scripts, with all parameters derived from datasheet or actual measurements. It is essential to note that loss analysis is a broad topic, and our simplified method only serves as a rough estimate of loss distribution, offering suggestions for efficiency improvement.

The author has uploaded the attachments "[LossEstimation.m](#)" and "[LossDistribution.m](#)" (directory: \SCH&SIMPLIS&MATLAB\MATLAB), serving as supporting materials. The estimated efficiency results are shown in Fig. A14.



(a). Efficiency in different load current.

(b). Input power in different output power.

Fig. A14. Efficiency curves of "[LossEstimation.m](#)".

Comparing the estimated results in Fig. A14 with the actual measured results in Fig. 23 in the paper, it is observed that they are reasonably consistent. This is evident in the following aspects:

- 1). The location of the highest efficiency point is consistently around 24 A (BCM point), and MBC efficiency starts declining after entering CCM (Continuous Conduction Mode).
- 2). The estimated results indicate that RAM losses remain constant.

As an example of optimizing peak efficiency, by setting $i_o = 24$ in "[LossDistribution.m](#)" and running the script, the loss distribution for an output current of 24A can be obtained, as illustrated in Fig. A15.

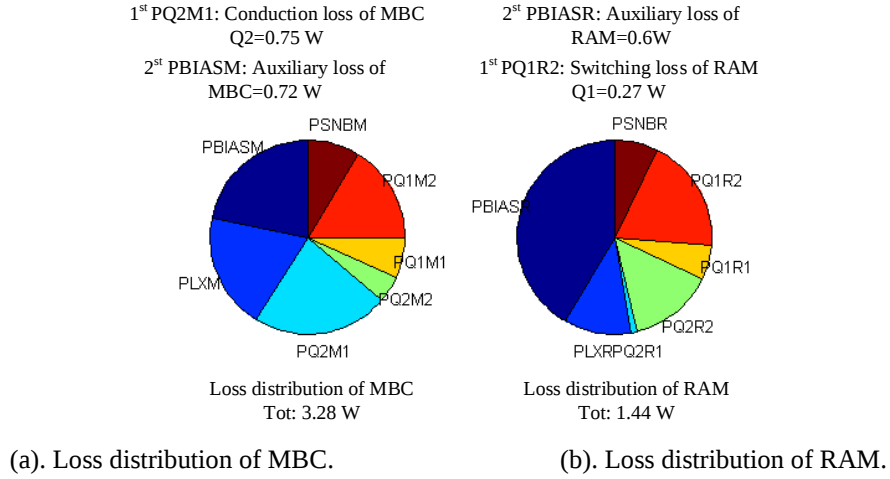


Fig. A15. Loss distribution of system at $I_o = 24$ A.

Based on the analysis results presented above, several measures can be taken:

- 1) For optimizing the efficiency of MBC, the focus should be on reducing the conduction loss of Q2.
- 2) To optimize the efficiency of RAM, the emphasis should be on reducing the P_{BIAS} loss. This can be achieved by replacing the LDO with a DC-DC converter in the auxiliary power supply.
- 3) Replacing the power inductor with a smaller ACR (AC resistance).

Efficiency was re-evaluated through measurements, and the peak efficiency of MBC increased from **86.6% to 88% ($I_o = 24$ A)**.

The efficiency curve has been redrawn and is presented in Fig. 23(a) of the paper, alongside Fig. 23(b).

Part.6 Inductance Mismatch

6.1 Influence of Inductance Mismatch on Output Current Ripple

γ is defined as the current compensation rate, which represents the ratio of compensated current ripple to uncompensated current ripple, as shown in Eq. (A33).

$$\gamma = \left| \frac{\Delta i_{sum} + \Delta i_{ax}}{\Delta i_{sum}} \right| = \left| \frac{T_{effon}(k_{rr} + k_{axd})}{\Delta i_{sum}} \right| \quad (A33)$$

Substituting Eq. (5) and Eq. (10) into Eq. (A33), and combining the voltage relationship: $V_o = DV_i$, Eq. (A34) can be obtained after eliminating T_{effon} , where β represents the ratio of inductances, and $\beta = L_{ax}/L$.

$$\gamma = \left| 1 - \frac{1}{\beta} \right| \quad (A34)$$

Eq. (A34) shows that when the inductance L_{ax} is infinite, β is infinite, $\gamma = 1$, and the RAM is not inserted. When the inductance $L_{ax} = L$, $\beta = 1$ and $\gamma = 0$, inserting RAM works perfectly. When the inductance $L_{ax} \ll L$, $\gamma \gg 1$, inserting RAM will even deteriorate the output current ripple of MBC.

6.2 Simulation Results

Eq. (A34) has been validated through simulation, as shown in Fig. 1.

The author has uploaded the attachments "[20231203mismatch](#)", serving as supporting materials. (directory: \SCH&SIMPLIS&MATLAB\SIMPLIS SIMULATION\InductanceMismatch)

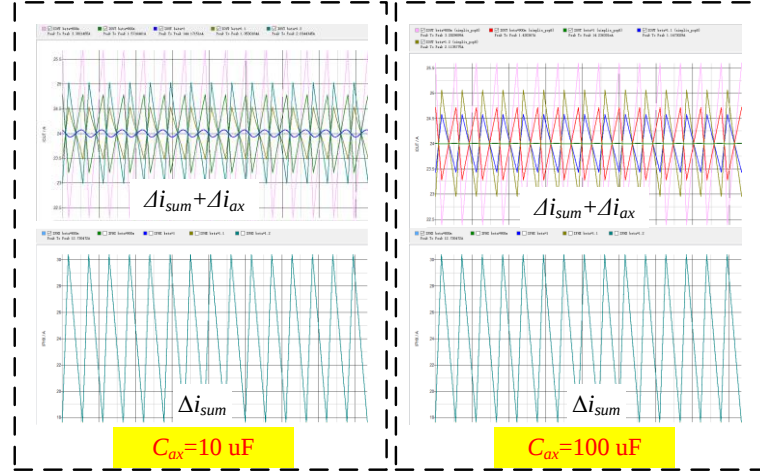


Fig. 1 The simulation results of inductance mismatch.

The simulation results are summarized in Table. AII.

Table. AII.

β	0.8	0.9	1.0	1.1	1.2
γ $C_{ax}=10$ uF	0.27	0.12	0.01	0.08	0.16
γ $C_{ax}=100$ uF	0.25	0.11	0.00	0.09	0.17
calculated γ	0.25	0.11	0	0.09	0.17

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Lastly, I extend my appreciation to my own passion for PEs, as it has been the driving force that kept me dedicated throughout the year.

Welcome to contact me by email if you have any doubts.

Sincerely
Jiazhe Chen